Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims

Claim 1 (Currently Amended): A multi-port cache memory, comprising:

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first to K-th N-port tag memories each ~~consisting of~~ comprising M-number of one-port cell blocks and of an N-port decoder for decoding ~~the~~ N cache line indices, each of the cache line indices having 1 bit or more, supplied to the first to K-th tag memories, each of K and M being an integer of 1 or more and N being an integer of more than 1;

first to K-th N-port data memories each comprising ~~consisting of~~ M-number of one-port cell blocks and of an N-port decoder for decoding the N cache line indices, each of the cache line indices having 1 bit or more, and the N cache line offsets[[,]] ~~each having 0 bit or more~~[[,]] supplied to the first to K-th data memories, each of the cache line offsets having 0 bits or more; and

a conflict management circuit for managing ~~the~~ write and read conflicts in the first to K-th N-port tag memories and the first to K-th N-port data memories.

Claim 2 (Currently Amended): The multi-port cache memory according to claim 1, wherein a cache line index ~~consists of~~ comprises a first cache line index for identifying the contents of any one or any plurality of the M-number of one-port cell blocks and a second cache line index for selecting any one or any plurality of the M-number of one-port cell blocks.

Claim 3 (Currently Amended): The multi-port cache memory according to claim 1, wherein the multi-port cache memory comprises first to K-th comparing circuits for

comparing ~~the~~ tags supplied to the first to K-th N-port tag memories with ~~the~~ tags generated from the first to K-th N-port tag memories, respectively, and a cache hit signal is transmitted for each of the N ports by supplying the outputs of the first to K-th comparing circuits to a K-input OR circuit for each of the N ports.

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Claim 4 (Currently Amended): The multi-port cache memory according to claim 1, wherein the number M of said one-port cell blocks is less than the number N of ports of said N-port tag ~~memory~~ memories and said N-port data ~~memory~~ memories.

Claim 5 (Currently Amended): The multi-port cache memory according to claim 1, wherein corresponding pairs of said N-port tag memories and said N-port data memories are combined to form combined N-port tag-data memories, and the word length of said combined N-port tag-data memories is represented by "mtag + $W*2^{mword}$" where mtag represents the number of bits of ~~the~~ an address allocated to ~~the~~ a tag, mword represents the number of bits of the address[[,]] ~~being 0 or more~~[[,]] allocated to ~~the~~ a cache line offset, mword being 0 or more, and W represents the word length of an instruction or a data word.

Claim 6 (Currently Amended): The multi-port cache memory according to claim 1, wherein said cell blocks included in said N-port tag ~~memory~~ memories and said N-port data ~~memory~~ memories ~~consist of~~ comprise L-port cell blocks having the number L of ports not less than 1 and less than N ($1 \leq L < N$, L being an integer).

Claim 7 (Currently Amended): The multi-port cache memory according to claim 1, wherein said tag ~~memory~~ memories ~~consists of~~ comprise L_{tag}-port cell blocks having the number L_{tag} of ports (L_{tag} being an integer not less than one), and said data ~~memory~~ memories

~~consists of~~ comprise L_{data}-port cell blocks having the number L_{data} of ports (L_{data} being an integer not less than one and differing from L_{tag}).

Claim 8 (Currently Amended): The multi-port cache memory according to claim 2, wherein said multi-port cache memory comprises first to K-th comparing circuits for comparing ~~the~~ tags supplied to the first to K-th N-port tag memories with ~~the~~ tags generated from the first to K-th N-port tag memories, respectively, and a cache hit signal is transmitted for each of the N ports by supplying the outputs of the first to K-th comparing circuits to a K-input OR circuit for each of the N ports.

Claim 9 (Currently Amended): The multi-port cache memory according to claim 2, wherein the number M of said one-port cell blocks is less than the number N of ports of said N-port tag ~~memory~~ memories and said N-port data ~~memory~~ memories.

Claim 10 (Currently Amended): The multi-port cache memory according to claim 2, wherein corresponding pairs of said N-port tag memories and said N-port data memories are combined to form combined N-port tag-data memories, and the word length of said combined N-port tag-data memories is represented by "mtag + $W*2^{mword}$" where mtag represents the number of bits of ~~the~~ an address[[,]] allocated to ~~the~~ a tag, mword represents the number of bits of ~~the~~ an address[[,]] ~~being 0 or more~~[[,]] allocated to ~~the~~ a cache line offset, mword being 0 or more, and W represents the word length of an instruction or a data word.

Claim 11 (Currently Amended): The multi-port cache memory according to claim 2, wherein said cell blocks included in said N-port tag ~~memory~~ memories and said N-port data

~~memory~~ memories ~~consists of~~ comprise L-port cell blocks having the number L of ports not less than 1 and less than N ($1 \leq L < N$, L being an integer).

Claim 12 (Currently Amended): The multi-port cache memory according to claim 2, wherein said tag ~~memory~~ memories ~~consists of~~ comprise L_{tag}-port cell blocks having the number L_{tag} of ports (L_{tag} being an integer not less than one), and said data ~~memory~~ memories ~~consists of~~ comprise L_{data}-port cell blocks having the number L_{data} of ports (L_{data} being an integer not less than one and differing from L_{tag}).

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Claim 13 (Currently Amended): The multi-port cache memory according to claim 3, wherein the outputs of said first to K-th comparing circuits control first to K-th enable circuits that permit the input and output of ~~the~~ write data and read data in and out of said first to K-th data memories.

Claim 14 (Currently Amended): The multi-port cache memory according to claim 3, wherein the number M of said one-port cell blocks is less than the number N of ports of said N-port tag ~~memory~~ memories and said N-port data ~~memory~~ memories.

Claim 15 (Currently Amended): The multi-port cache memory according to claim 3, wherein corresponding pairs of said N-port tag memories and said N-port data memories are combined to form combined N-port tag-data memories, and the word length of said combined N-port tag-data memories is represented by "mtag + $W*2^{mword}$" where mtag represents the number of bits of the address allocated to the tag, mword represents the number of bits of ~~the~~ an address[[,]] ~~being 0 or more~~[[,]] allocated to ~~the~~ a cache line offset, mword being 0 or more, and W represents the word length of an instruction or a data word.

Claim 16 (Currently Amended): The multi-port cache memory according to claim 3, wherein said cell blocks included in said N-port tag ~~memory~~ memories and said N-port data ~~memory~~ memories ~~consists of~~ comprise L-port cell blocks having the number L of ports not less than 1 and less than N ($1 \leq L < N$, L being an integer).

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Claim 17 (Currently Amended): The multi-port cache memory according to claim 3, wherein said tag ~~memory~~ memories ~~consists of~~ comprise L_{tag}-port cell blocks having the number Lt_{ag} of ports (Lt_{ag} being an integer not less than one), and said data ~~memory~~ memories ~~consists of~~ comprise L_{data}-port cell blocks having the number L_{data} of ports (L_{data} being an integer not less than one and differing from L_{tag}).

Claim 18 (Currently Amended): The multi-port cache memory according to claim 8, wherein the outputs of said first to K-th comparing circuits control first to K-th enable circuits that permit the input and output of ~~the~~ write data and read data in and out of said first to K-th data memories.

Claim 19 (Currently Amended): The multi-port cache memory according to claim 8, wherein the number M of said one-port cell blocks is less than the number N of ports of said N-port tag ~~memory~~ memories and said N-port data ~~memory~~ memories.

Claim 20 (Currently Amended): The multi-port cache memory according to claim 8, wherein corresponding pairs of said N-port tag memories and said N-port data memories are combined to form combined N-port tag-data memories, and the word length of said combined N-port tag-data memories is represented by "mtag + $W*2^{mword}$" where mtag represents the

number of bits of ~~the~~ an address allocated to ~~the~~ a tag, mword represents the number of bits of ~~the~~ an address~~, being 0 or more,~~ allocated to the cache line offset, mword being 0 or more, and W represents the word length of an instruction or a data word.

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Claim 21 (Currently Amended): The multi-port cache memory according to claim 8, wherein said cell blocks included in said N-port tag ~~memory~~ memories and said N-port data ~~memory~~ memories ~~consist of~~ comprise L-port cell blocks having the number L of ports not less than 1 and less than N ($1 \leqq L < N$, L being an integer).

Claim 22 (Currently Amended): The multi-port cache memory according to claim 8, wherein said tag ~~memory~~ memories ~~consists of~~ comprise L_{tag}-port cell blocks having the number L_{tag} of ports (L_{tag} being an integer not less than one), and said data ~~memory~~ memories ~~consists of~~ comprise L_{data}-port cell blocks having the number L_{data} of ports (L_{data} being an integer not less than one and differing from L_{tag}).

Claim 23 (Currently Amended): The multi-port cache memory according to claim 13, wherein the number M of said one-port cell blocks is less than the number N of ports of said N-port tag ~~memory~~ memories and said N-port data ~~memory~~ memories.

Claim 24 (Currently Amended): The multi-port cache memory according to claim 13, wherein corresponding pairs of said N-port tag memories and said N-port data memories are combined to form combined N-port tag-data memories, and the word length of said combined N-port tag-data memories is represented by "mtag + $W*2^{mword}$" where mtag represents the number of bits of ~~the~~ an address allocated to ~~the~~ a tag, mword represents the

number of bits of ~~the~~ an address~~, being 0 or more,~~ allocated to ~~the~~ a cache line offset, mword being 0 or more, and W represents the word length of an instruction or a data word.

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Claim 25 (Currently Amended): The multi-port cache memory according to claim 13, wherein said cell blocks included in said N-port tag ~~memory~~ memories and said N-port data ~~memory~~ memories ~~consist of~~ comprise L-port cell blocks having the number L of ports not less than 1 and less than N ($1 \leq L < N$, L being an integer).

Claim 26 (Currently Amended): The multi-port cache memory according to claim 13, wherein said tag ~~memory~~ memories ~~consists of~~ comprise L_{tag}-port cell blocks having the number L_{tag} of ports (L_{tag} being an integer not less than one), and said data ~~memory~~ memories ~~consists of~~ comprise L_{data}-port cell blocks having the number L_{data} of ports (L_{data} being an integer not less than one and differing from L_{tag}).

Claim 27 (Currently Amended): The multi-port cache memory according to claim 18, wherein the number M of said one-port cell blocks is less than the number N of ports of said N-port tag ~~memory~~ memories and said N-port data ~~memory~~ memories.

Claim 28 (Currently Amended): The multi-port cache memory according to claim 18, wherein corresponding pairs of said N-port tag memories and said N-port data memories are combined to form combined N-port tag-data memories, and the word length of said combined N-port tag-data memories is represented by "mtag + $W*2^{mword}$" where mtag represents the number of bits of ~~the~~ an address allocated to ~~the~~ a tag, mword represents the number of bits of ~~the~~ an address~~, being 0 or more,~~ allocated to ~~the~~ a cache line offset, mword being 0 or more, and W represents the word length of an instruction or a data word.

Claim 29 (Currently Amended): The multi-port cache memory according to claim 18, wherein said cell blocks included in said N-port tag ~~memory~~ memories and said N-port data ~~memory~~ memories ~~consist of~~ comprise L-port cell blocks having the number L of ports not less than 1 and less than N ($1 \leq L < N$, L being an integer).

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Claim 30 (Currently Amended): The multi-port cache memory according to claim 18, wherein said tag ~~memory~~ memories ~~consists of~~ comprise L_{tag}-port cell blocks having the number L_{tag} of ports (L_{tag} being an integer not less than one), and said data ~~memory~~ memories ~~consists of~~ comprise L_{data}-port cell blocks having the number L_{data} of ports (L_{data} being an integer not less than one and differing from L_{tag}).

Claim 31 (Currently Amended): An N-port tag memory, comprising:

an M-number of one-port cell blocks, M being an integer of one or more;

a global switching network including a bus system, a crossbar switch or a multistage connection network, serving to impart N-port multi-port functions to the M-number of one-port cell blocks, N being an integer of more than one; and

connections for a conflict management circuit connected to control the global switching network~~, consisting, for example, of a bus system or a crossbar switch,~~ in the case of access conflicts between the N-ports,

wherein the outputs of a conflict management circuit ~~and~~, for each of the N ports, a first cache line index for identifying the contents of any one or any plurality of the M-number of one-port cell blocks, a second cache line index for selecting any one or any plurality of the M-number of one-port cell blocks, and a read/write instruction transmitted from a microcomputer core are supplied to at least the global switching network.

Claim 32 (Original): The N-port tag memory according to claim 31, wherein the number M of said one-port cell blocks is less than the number N of ports of said N-port tag memory.

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Claim 33 (Currently Amended): The N-port tag memory according to claim 31, wherein said N-port tag memory and an N-port data memory forming a pair with said N-port tag memory are combined to form a combined N-port tag-data memory, and the word length of said combined N-port tag-data memory is represented by "mtag + $W*2^{mword}$" where mtag represents the number of bits of ~~the~~ an address allocated to ~~the~~ a tag, mword represents the number of bits of ~~the~~ an address~~, being 0 or more,~~ allocated to ~~the~~ a cache line offset, mword being 0 or more, and W represents the word length of an instruction or a data word.

Claim 34 (Original): The N-port tag memory according to claim 31, wherein said cell blocks included in said N-port tag memory are L-port cell blocks having the number L of ports not less than 1 and less than N ($1 \leq L < N$, L being an integer).

Claim 35 (Currently Amended): The N-port tag memory according to claim 31, wherein said tag memory ~~consists of~~ comprises L_{tag}-port cell blocks having the number L_{tag} of ports (L_{tag} being an integer not less than one), and an N-port data memory forming a pair with said N-port tag memory ~~consists of~~ comprises L_{data}-port cell blocks having the number L_{data} of ports (L_{data} being an integer not less than one and differing from L_{tag}).

Claim 36 (Currently Amended): An N-port data memory, comprising:

an M-number of one-port cell blocks, M being an integer of one or more;

a global switching network including a bus system, a crossbar switch or a multistage connection network, serving to impart an N-port multi-port function to the M-number of one-port cell blocks, N being an integer of more than one; and

connections for a conflict management circuit connected to control the global switching network ~~consisting, for example, of a bus system or a crossbar switch,~~ in the case of conflicts between the N ports,

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wherein the outputs of a conflict management circuit, ~~and~~ for each of the N ports, a first cache line index for identifying the contents of any one or any plurality of the M-number of one-port cell blocks, a second cache line index for selecting any or any plurality of the M-number of one-port cell blocks, a cache line offset allowing the cache line to ~~consist of~~ comprise more than one data word, and a read/write instruction transmitted from a microcomputer core are supplied to at least the global switching network, and instructions or data words are transmitted to or from the global switching network.

Claim 37 (Original): The N-port data memory according to claim 36, wherein the number M of said one-port cell blocks is less than the number N of ports of said N-port data memory.

Claim 38 (Currently Amended): The N-port data memory according to claim 36, wherein said N-port data memory and an N-port tag memory forming a pair with said N-port data memory are combined to form a combined N-port tag-data memory, and the word length of said combined N-port tag-data memory is represented by "mtag + $W*2^{mword}$" where mtag represents the number of bits of ~~the~~ an address allocated to ~~the~~ a tag, mword represents the number of bits of ~~the~~ an address, ~~being 0 or more,~~ allocated to ~~the~~ a cache line offset, mword being 0 or more, and W represents the word length of an instruction or a data word.

Claim 39 (Original): The N-port data memory according to claim 36, wherein said cell blocks included in said N-port data memory are L-port cell blocks having the number L of ports not less than 1 and less than N ($1 \leqq L < N$, L being an integer).

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Claim 40 (Currently Amended): The N-port data memory according to claim 36, wherein a tag memory forming a pair with said data memory ~~consists of~~ comprises L_{tag}-port cell blocks having the number L_{tag} of ports (L_{tag} being an integer not less than one), and said data memory ~~consists of~~ comprises L_{data}-port cell blocks having the number L_{data} of ports (L_{data} being an integer not less than one and differing from L_{tag}).

Claim 41 (Currently Amended): An N-port tag memory, comprising:

an M-number of one-port cell blocks, M being an integer of one or more;

a port transition circuit for converting the function of the one-port cell block to the function of an N-port block, N being an integer more than one;

an M-number of N-port blocks the function of which has been obtained by mounting the port transition circuit to each of the M-number of one-port cell blocks;

a circuit network performing the address decoding function for N-ports to be connected to the M-number of N-port blocks; and

connections for a conflict management circuit to control in case of an access conflict the circuit network performing the address decoding function for the M-number of N-port blocks;

wherein, for each of the N ports, a first cache line index for identifying the contents of any one or any plurality of the M-number of one-port cell blocks[[,]]and a read/write instruction from a microcomputer are supplied to at least the port transition circuit[[s,]] and

the outputs of a conflict management circuit, and, again for each of the N ports, a second cache line index for selecting any one or any plurality of the M-number of one-port cell blocks[[,]] and a read/write instruction from a microcomputer core are supplied to at least the circuit network performing the address decoding function for the M-number of N-port blocks.

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Claim 42 (Original): The N-port tag memory according to claim 41,

wherein the number M of said one-port cell blocks is less than the number N of ports of said N-port tag memory.

Claim 43 (Currently Amended): The N-port tag memory according to claim 41, wherein said N-port tag memory and an N-port data memory forming ~~or~~ a pair with said N-port tag memory are combined to form a combined N-port tag-data memory, and the word length of said combined N-port tag-data memory is represented by "mtag + $W*2^{mword}$" where mtag represents the number of bits of ~~the~~ an address allocated to ~~the~~ a tag, mword represents the number of bits of ~~the~~ an address~~, being 0 or more,~~ allocated to the cache line offset, mword being 0 or more, and W represents the word length of an instruction or a data word.

Claim 44 (Currently Amended): The N-port tag memory according to claim 41, wherein said N-port blocks included in said N-port tag memory ~~consist of~~ comprise L-port cell blocks having the number L of ports not less than 1 and less than N ($1 \leq L < N$, L being an integer), and a port transition circuit for converting the function of the L-port cell block to the function of the N-port block.

Claim 45 (Currently Amended): An N-port data memory, comprising:

an M-number of one-port cell blocks, M being an integer of one or more;

a port transition circuit for converting the function of the one-port cell block to the function of an N-port block, N being an integer more than one;

an M-number of N-port blocks the function of which has been obtained by mounting the port transition circuit to each of the M-number of one-port cell blocks;

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a circuit network performing the address decoding function for N-ports to be connected to the M-number of N-port blocks; and

connections for a conflict management circuit to control in case of an access conflict the circuit network performing the address decoding function for the M-number of N-port blocks,

wherein, for each of the N ports, a first cache line index for identifying the contents of any one or any plurality of the M-number of one-port cell blocks, a cache line offset allowing the cache line to ~~consist of~~ comprise more than one data word, and a read/write instruction from a microcomputer are supplied to at least the port transition ~~circuits,~~ circuit and the outputs of a conflict management circuit, and, again for each of the N ports, a second cache line index for selecting any one or any plurality of the M-number of one-port cell blocks[[,]] and a read/write instruction from a microcomputer core[[,]] are supplied to at least the circuit network performing the address decoding function for the M-number of N-port blocks, and data words or instructions are transmitted to or from the circuit network performing the address decoding function of the M-number of N-port blocks.

Claim 46 (Original): The N-port data memory according to claim 45, wherein the number M of said one-port cell blocks is less than the number N of ports of said N-port data memory.

Claim 47 (Currently Amended): The N-port data memory according to claim 45, wherein an N-port tag memory forming a pair with said N-port data memory and said N-port data memory are combined to form a combined N-port tag-data memory, and the word length of said combined N-port tag-data memory is represented by "mtag + $W*2^{mword}$" where mtag represents the number of bits of ~~the~~ an address allocated to ~~the~~ a tag, mword represents the number of bits of ~~the~~ an address~~, being 0 ore more,~~ allocated to ~~the~~ a cache line offset, mword being 0 or more, and W represents the word length of an instruction or a data word.

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Claim 48 (Currently Amended): The N-port data memory according to claim 45, wherein said N-port blocks included in said N-port data memory ~~consist of~~ comprise L-port cell blocks having the number L of ports not less than 1 and less than N ($1 \leq L < N$, L being an integer), and a port transition circuit for converting the function of the L-port cell block to the function of the N-port block.

Claim 49 (Currently Amended): An N-port tag memory, comprising:

an M_B-number of one-port cell blocks, where M_B is represented by $M*M_S$, each of M_S and M being an integer of one or more;

an M_S-number of global switching networks, each including a bus system, a crossbar switch or a multistage interconnection network, each serving to impart N-port multi-port functions to an M-number of one-port cell blocks, N being an integer of more than one; and

an M_S-number of connections for conflict management circuits connected to control the global switching networks~~, consisting, for example, of a bus system or a crossbar switch,~~ in the case of access conflicts between the N-ports,

wherein the outputs of a conflict management circuit ~~and~~, for each of the N ports, a first cache line index for identifying the contents of any one or any plurality of the M-number

of one-port cell blocks, a second cache line index for selecting any one or any plurality of the M-number of one-port cell blocks, and a read/write instruction transmitted from a microcomputer core are supplied to at least each of the global switching networks.

Claim 50 (Currently Amended): An N-port data memory, comprising:

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an M_B-number of one-port cell blocks, where M_B is represented by $M*M_S$, each of M_S and M being an integer of one or more;

an M_S-number of global switching networks, each including a bus system, a crossbar switch or a multistage interconnection network, each serving to impart an N-port multi-port function to an M-number of one-port cell blocks, N being an integer of more than one; and

an MS-number of connections for conflict management circuits connected to control the global switching networks ~~consisting, for example, of a bus system or a crossbar switch,~~ in the case of conflicts between the N ports,

wherein the outputs of a conflict management circuit, ~~and~~ for each of the N ports, a first cache line index for identifying the contents of any one or any plurality of the M-number of one-port cell blocks, a second cache line index for selecting any one or any plurality of the M-number of one-port cell blocks, a cache line offset allowing the cache line to ~~consist of~~ comprise more than one data word, and a read/write instruction transmitted from a microcomputer core are supplied to at least each of the global switching networks, and instructions or data words are transmitted to or from each of the global switching networks.

Claim 51 (Currently Amended): An N-port tag memory, comprising:

an M_B-number of one-port cell blocks, where M_B is represented by $M*M_S$, each of M_S and M being an integer of one or more;

a port transition circuit for converting the function of the one-port cell block to the function of an N-port block, N being an integer more than one;

an M_B-number of N-port blocks the function of which has been obtained by mounting the port transition circuit to each of the M_B-number of one-port cell blocks;

an M_S-number of circuit networks performing the address decoding function for N-ports to be connected to an M-number of N-port blocks; and

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an M_S-number of connections for conflict management circuits to control in case of an access conflict the respective circuit network performing the address decoding function for the M-number of N-port blocks;

wherein, for each of the N ports, a first cache line index for identifying the contents of any one or any plurality of the M-number of one-port cell blocks, and a read/write instruction from a microcomputer are supplied to at least each of the port transition circuits[[,]] and the outputs of a conflict management circuit, and, again for each of the N ports, a second cache line index for selecting any one or any plurality of the M-number of one-port cell blocks[[,]] and a read/write instruction from a microcomputer core are supplied to at least each of the circuit networks performing the address decoding function for the M-number of N-port blocks.

Claim 52 (Currently Amended): An N-port data memory, comprising:

an M_B-number of one-port cell blocks, where M_B is represented by $M*M_S$, each of M_S and M being an integer of one or more;

a port transition circuit for converting the function of the one-port cell block to the function of an N-port block, N being an integer more than one;

an M_B-number of N-port blocks the function of which has been obtained by mounting the port transition circuit to each of the M_B-number of one-port cell blocks;

an M_S-number of circuit networks performing the address decoding function for N-ports to be connected to an M-number of N-port blocks; and

an M_S-number of connections for conflict management circuits to control in case of an access conflict the respective circuit network performing the address decoding function for the M-number of N-port blocks,

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wherein, for each of the N ports, a first cache line index for identifying the contents of any one or any plurality of the M-number of one-port cell blocks, a cache line offset allowing the cache line to ~~consist of~~ comprise more than one data word, and a read/write instruction from a microcomputer are supplied to at least each of the transition circuits[[,]] and the outputs of a conflict management circuit, and, again for each of the N ports, a second cache line index for selecting any one or any plurality of the M-number of one-port cell blocks[[,]] and a read/write instruction from a microcomputer core[[,]] are supplied to at least each of the circuit networks performing the address decoding function for the M-number of N-port blocks, and data words or instructions are transmitted to or from each of the circuit networks performing the address decoding function of the M-number of N-port blocks.